Center of Excellence DEWS & Thales Alenia Space Italia present:

From **Plural** to **MacSpace**

**Prof. Ran Ginosar**  
EE & CS, Technion and Ramon Chips, Israel

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**Abstract:** The *Plural* many-core architecture combines many small cores, many shared memory banks, a hardware scheduler, and two custom active networks-on-chip: cores-to-memories and cores-to-scheduler. A theoretical model (almost) justifies increasing the number of cores while making them smaller and slower, maximizing performance-to-power ratio. Several benchmark simulations are demonstrated, showing close to linear speedup and high performance-to-power ratio. *Many-Flow*, a de-synchronized PRAM-like task-based non-CSP and non-locking programming model for shared memory, enables fine-grain parallelism. *MacSpace* (http://www.macspace.eu/), a rad-hard 64-core version, is implemented in silicon. A software development environment for MacSpace is shown, enabling fast and convenient investigation of applications on a personal computer.

**Bio:** Prof. Ran Ginosar received BSc from the Technion and PhD from Princeton University. He has conducted research at Bell Laboratories, the University of Utah and Intel Research Laboratories in Oregon, USA. He is member of the faculty of EE and CS departments at the Technion, and heads the VLSI Systems Research Center. He has also co-founded several start-up companies in the area of VLSI and parallel processing. He is the founder and CEO of Ramon Chips, a rad-hard semiconductor company. His research interests focus on VLSI, asynchronous logic and parallel processing architectures.

*Please, register by sending an email to: luigi.pomante@univaq.it*